REMARKS

The Office Action dated January 29, 2004, has been received and carefully considered. Claims 1-17, 19, 20, and 22-24 are pending in the present application. In this response, claims 9, 13, 16, 19, 20, 22 and 23 have been amended and claim 21 has been cancelled without prejudice. Support for the amendments to the claims may be found in the specification and figures as originally filed. Entry of the amendments to the claims therefore is respectfully requested. Reconsideration of the outstanding objections and rejections in the present application is further respectfully requested based on the following remarks.

The Objection to Claims 13, 19, 21 and 23

At page 2 of the Office Action, claims 13, 19, 21 and 23 were objected to for various informalities. The Applicants have amended claims 13, 19, 21 and 23 consistent with the Examiner's comments. The Applicants therefore respectfully request that this objection be withdrawn.

The Anticipation Rejection of Claims 1-12

At pages 3-6 of the Office Action, claims 1-12 were rejected under 35 U.S.C. § 102(e) as being anticipated by Hassoun (U.S. Patent No. 6,487,648). This rejection is hereby respectfully traversed.

> With respect to claim 1, the Examiner alleges that Hassoun teaches:
>
> a. receiving a first clock (CLK_FB) [figure 5]; b. providing a distributed clock signal (CLK_SD) to a clock distribution network having a plurality of endpoints (CLK_SD is distributed to different memory devices) connected to a respective plurality of components (SDRAM 308 and 309) [figure 5]; and c. modifying the distributed clock signal (by Delay Lock Loop 304) until a portion the distributed clock signal received at the first end of the plurality of endpoints point [SIC] (CLK_SD at the input to SDRAMS 308 and 309) is substantially synchronized to the first clock signal (*the first clock and distributed clock signals are substantially synchronized because they are the same node*) [figures 4 and 5].

Office Action, page 3, section 8 (emphasis added).

Thus, the Examiner asserts that Hassoun teaches modifying the clock signal CLK_SD such that it is substantially synchronized to the clock signal CLK_FB and Hassoun therefore discloses the invention recited by claim 1. However, one of ordinary skill in the art will appreciate that CLK_SD and CLK_FB represent the same clock signal, and as such, are always synchronized. *See, e.g.,* Hassoun, col. 10, lines 15-21 (teaching that the "[s]kewed clock signal S_CLK [i.e., CLK_SD] is also fed back to a feedback terminal FB of DLL 304 [as CLK_FB]"). The Examiner also recognizes that the signals CLK_SD and CLK_FB are the same signal, as the Examiner states that "the first clock and distributed clock signals are substantially synchronized because they are at the same node." Office Action, p. 3. Being the same signal, there is no need to modify the distributed clock signal CLK_SD to be synchronized with the clock signal CLK_FB. In fact, the modification of the clock signal CLK_SD simply results in a corresponding modification to the clock signal CLK_FB, which may result in a race condition at the DLL 304 of Hassoun. Accordingly, not only does Hassoun fail to disclose or even suggest the limitations of modifying the distributed clock signal until a portion of the distributed clock signal received at an endpoint is substantially synchronized to a first clock signal as recited in claim 1, Hassoun teaches away from the invention recited in claim 1 as such a modification in the system of Hassoun would be ineffective at best and counter-productive at worst.

Accordingly, Hassoun and the other cited references fail to disclose or suggest, alone or in combination, each and every limitation recited in claim 1. Hassoun and the other cited references therefore fail to disclose or suggest each and every limitation recited in claims 2-12 at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features that are not disclosed or even suggested by the cited references taken either alone or in combination. For example, claim 6 recites the limitations of providing a second clock signal (where the first clock signal is a delayed representation of the second clock signal) manufactured onto a propagation path of a first substrate separate from the first device. Neither Hassoun nor the other cited references disclose the provision of a signal to such a propagation path.

In view of the foregoing, it is respectfully submitted that the anticipation rejection of claims 1-12 is improper at this time and the withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejection of Claims 13 and 14

At pages 3 and 6-8 of the Office Action, claims 13 and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hassoun (U.S. Patent No. 6,587,534). This rejection is hereby respectfully traversed.

The Examiner alleges that Hassoun teaches each and every limitation recited in claims 13 and 14. In particular, with respect to claim 13, the Examiner alleges that Hassoun teaches the limitations of: 1) "providing a representation of a first clock signal to a delay element (delay elements such as clock buffers, not explicitly shown but suggested as existing in clock skew 180) [figures 1 and 3, col. 1 lines 55 through col. 2 line 4 and col. 5 lines 24-49]." Office Action, p. 6; and 2) "providing a representation (clock skew containing delay from a group of devices and elements including representation of all the leaves) of the delayed clock signal (at terminal 306) from the leaves (wherein a leaf is interpreted to [be] one of the logic circuits 190) to the delay element (wherein the leaves are the logic circuits)." Office Action, p. 7.

The Applicants respectfully submit that, contrary to the Examiner's assertions, Hassoun fails to disclose or suggest at least these limitations. With respect to the limitations of providing a representation of the delayed clock signal from a first leaf to the delay element, it is respectfully submitted that the Examiner fails to demonstrate that Hassoun discloses providing a representation of the delayed clock signal from the logic circuits 190 (which the Examiner equates to the first leaf of the clock distribution tree) to the clock skew 180 (which the Examiner equates to the delay element of claim 13). Regardless of whether the clock skew 180 is equivalent to the delay element of claims 13 and 14, neither the figures nor the written description of Hassoun disclose or suggest the provision of any type of signal, much less a representation of a clock signal, from the logic circuits 190 to any element of the clock skew 180.

With respect to the provision of a representation of the first clock signal to a delay element, the Examiner inaccurately equates clock buffers (which may exist in clock skew 180) of

Hassoun to a delay element as recited in claims 13 and 14. However, as is understood from the context of claim 13 and from the teachings of the present application, the delay element of claims 13 and 14 intentionally inserts a delay in the resulting delayed clock signal to assist in synchronization of the clock signal, whereas the delay introduced by clock skew 180, including the delay caused by clock buffers, is described in Hassoun as clock skew, which indicates that the resulting delay is unintentional or a by-product.

Accordingly, Hassoun and the other cited references fail to disclose or suggest, alone or in combination, each and every limitation recited in claim 1. Hassoun and the other cited references therefore also fail to disclose or suggest, alone or in combination, each and every limitation recited in claim 14 at least by virtue of its dependency on claim 13. Moreover, claim 14 recites additional limitations that are not disclosed or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully submitted that the obviousness rejection of claims 13 and 14 is improper at this time and the withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejection of Claims 15-17 and 19-24

At pages 8-15 of the Office Action, claims 15-17 and 19-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen (U.S. Patent No. 6,003,118). This rejection is hereby respectfully traversed.

A) Claims 15-17

With respect to independent claim 15, the Examiner alleges that Chen teaches each and every limitation recited, except that Chen does not expressly disclose providing a representation of the first clock to a delay component of the first device, wherein the representation of the first clock is approximately equal to the first clock delayed by an amount approximately equal to the sum of the first second and third propagation delays. Office Action, pp. 8-10. In particular, the Examiner alleges that Chen discloses the limitations of providing a representation of a first clock to a delay component (which the Examiner equates to the load 256 of Chen), wherein the representation of the first clock is approximately equal to the first clock delayed by an amount

approximately equal to the sum of the first, second and third propagation delays (which the Examiner equates to the phase lead and phase lag taught by Chen to compensate for phase differences between clock signals at the memory module, read data buffer and write buffer). Office Action, p. 9.

Applicants respectfully disagree that Chen discloses or even suggests the limitations of providing a representation of the first clock to a delay component, wherein the representation of the first clock *is approximately equal to the first clock delayed by an amount approximately equal to the sum of the first, second and third delays* as presently recited by independent claim 15. With respect to these limitations, the Examiner cites Figure 2A and col. 4, lines 31-39 and col. 8, lines 15-21 of Chen in support of Chen's alleged disclosure of these limitations. Office Action, p. 9. However, none of the cited passages of Chen, nor any other passage of Chen, disclose or even suggest the provision of a representation of a clock signal that is equivalent to the clock signal delayed by the sum of the first, second and third propagation delays as described and claimed in the present application. As an initial issue, the clock synchronization techniques disclosed in Chen fail to take into account the propagation delay of the data signal generated by the memory. In contrast, claim 15 recites the provision of a representation of a clock signal that has been delayed by a time period that includes a propagation delay resulting from the generation of a data signal generated in response to the reception of a clock signal at a second device. Moreover, Chen merely discloses synchronization means for generating a memory clock signal where the memory clock signal has a phase lead relative to a memory read clock signal and a phase lag relative to a memory write clock signal. *See, e.g.*, Chen, claim 1. Thus, Chen describes a memory clock signal that leads a read clock signal and lags a write clock signal and fails to contemplate a memory clock signal delayed for a time period substantially equivalent to the sum of the propagation delays resulting from the provision of the read signal to the memory and resulting during the provision of the write signal.

Additionally, the Examiner, in addressing the distinction between having the delay component on the first device or separate from the first device, asserts that the synchronization means 23 of Figure 2A of Chen would render it "obvious to one of ordinary skill in the art at the time of the invention to modify Chen by having the synchronization means with the delay component and clock driver for clock distribution on the microcontroller because Chen suggests

doing so." Office Action, p. 10. The distinction between the load 256 of Chen and the delay component of the present invention notwithstanding, it is respectfully submitted that the illustration of a general "synchronization means" as part of the memory controller of Chen does not inherently lend itself to the conclusion that the inclusion of a delay component as part of the memory component is inherent to the disclosure of Chen. In fact, as the Examiner states with respect to the rejection of claim 21, "[b]ecause the load [256] is a device an artisan would have recognized that is should be on a substrate different from the first trace to more accurately simulate the behavior of the memory module." Office Action, p. 14. Thus, according to the Examiner, the load 256 should be on a separate substrate to more accurately simulate a memory device, which is also on a separate substrate. Therefore it would not be obvious to include or incorporate the load 256 on or with the first device.

As demonstrated above, Chen and the other cited references fail to disclose or even suggest, alone or in combination, each and every recited limitation of claim 15. Claims 16 and 17 depend from claim 15 and Chen and the other cited reference therefore fail to disclose or suggest the limitations recited in these claims at least by virtue of their dependency on claim 15. Moreover, claims 16 and 17 recite additional limitations that are not disclosed or suggested by the cited references taken either alone or in combination.

B) Claims 19-22

Claim 20 has been amended to further recite the limitations of: a second output port having an output node connected to a second trace, wherein the second output port is formed on a first substrate, and the second trace is formed on the second substrate; a *storage device* having an input coupled to the second trace and a *data output* coupled to a third trace, wherein the *storage device* is formed on a third substrate which is different from the second substrate and the third trace is formed on the second substrate; and the first input port having an input node connected to the third trace, and an output node coupled to an input of one of the plurality of components. Support for the amendments to Claim 20 may be found, *inter alia*, in original claims 20 and 21 and in Figure 2A (e.g., elements 40 and 47) and its corresponding description as originally filed. No new matter is introduced by these amendments.

It is respectfully submitted that Chen fails to disclose at least the limitations of a *storage*

device having an input coupled to the second trace and a *data output* coupled to a third trace, wherein the *storage device* is formed on a third substrate which is different from the second substrate and the third trace is formed on the second substrate, and the first input port having an input node connected to the third trace, and an output node coupled to an input of one of the plurality of components. Addressing original claim 21, from which these limitations are based, the Examiner alleged that load 256 of Chen is equivalent to a second device and "is used to simulate the effect of the memory module." The Examiner then concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Chen by placing the load [256] on a third substrate to simulate the effect of the memory module." Office Action, p. 14. However, claim 20 presently recites a storage device (e.g., a memory module) formed on the third substrate and having a data output. It will be appreciated that load 256 of Chen is not nor is it intended to be a storage device and, as such, does not have a data output. Instead, the load 256 of Chen only simulates the effect of the memory module as admitted by the Examiner. As neither the load 256 nor any other component of the systems disclosed in Chen are configured or connected as recited in claim 20, Chen fails to disclose or suggest the limitation of a storage device coupled as recited in claim 20.

Accordingly, Chen and the other cited references fail to disclose or suggest, alone or in combination, each and every limitation recited in claim 20. Chen and the other cited references therefore fail to disclose or even suggest each and every limitation of claims 19 and 22 at least by virtue of their dependency from claim 20. Moreover, claims 19 and 22 recite additional limitations that are not disclosed or even suggested by the cited references taken either alone or in combination. To illustrate, claim 22 recites the additional limitations of wherein the first trace is at least as long as the sum of the lengths of the second and third traces. These limitations were not addressed by the Examiner in the present Office Action and it is respectfully submitted that Chen and the other references fail to contemplate the respective lengths of such traces.

C) Claims 23 and 24

With respect to independent claim 23, the Examiner alleges that Chen discloses each and every recited limitation except the limitation that the delay component be a part of the first device. In particular, the Examiner asserts that Chen discloses the limitations of: receiving a third signal at a storage component in response to the first clock signal, wherein a latching signal

is based upon the modified second clock signal and a previous latching signal from the delay component; and latching the third signal at the storage component based upon the latching signal. The Applicants respectfully submit that Chen provides no support for the Examiner's allegations with regard to these limitations. The Examiner asserts that the latching signal, which the Examiner equates to signal 215, is based on CLK_L and the previous latching signal is equivalent to CLK_M from through the PLL. The Examiner further asserts that the limitation of latching the third signal at the storage component based upon the latching signal is disclosed by Chen as data is latched at node 244. Office Action, p. 15.

The Applicants respectfully submit that the Examiner's description of the system of Chen is inaccurate. The latching signal 215 used by the read data buffer 246 of Chen is not based on a modified clock signal and a previous latching signal from a delay component as recited in claim 23. Instead, as demonstrated by Figure 2B of Chen, the latching signal 215 is based solely on the reference signal provided by the clock generator 200 as modified by the PLL 206 and phase delay element 208. Contrary to the Examiner's description of Chen, the clock signal CLK_L, which the Examiner equates to the modified second signal, is not input to the PLL 206 or the phase delay element 208 and thus has no impact on the modification of the latching signal 215. Similarly, the clock signal CLK_M, which the Examiner equates to the previous latching signal, is not input to the PLL 206 or the phase delay element 208 and therefore does not affect or cause any modification of the latching signal 215. Accordingly, Chen fails to disclose or suggest at least the limitations of latching a third signal using a latching signal that is based upon a modified second clock signal and a previous latching signal from a delay component as recited in claim 23.

Accordingly, Chen and the other cited references fail to disclose each and every limitation recited in claim 23. Chen and the other cited references therefore fail to disclose or even suggest the recited limitations of claim 24 at least by virtue of its dependency from claim 23. Moreover, claim 24 recites additional limitations that are not disclosed or suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully submitted that the obviousness rejection of claims 15-17 and 19-24 is improper at this time and the withdrawal of this rejection therefore is

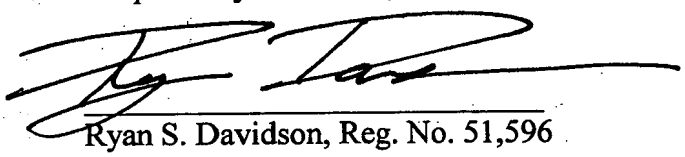
respectfully requested.

Conclusion:

It is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

Applicants believe no additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-0441.

Respectfully submitted,



April 29, 2004
Date

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